ABSTRACT OF THE DISCLOSURE

ELECTRICALLY ERASABLE AND PROGRAMMABLE NON-VOLATILE MEMORY CELL

An electrically erasable and programmable memory cell is provided. The memory cell includes a floating gate MOS transistor and a bipolar transistor for injecting an electric charge into the floating gate. The floating gate transistor has a source region and a drain region formed in a first well with a channel defined between the drain and source regions, a control gate region, and a floating gate extending over the channel and the control gate region. The bipolar transistor has an emitter region formed in the first well, a base region consisting of the first well, and a collector region consisting of the channel. The memory cell includes a second well that is insulated from the first well, and the control gate region is formed in the second well. Further embodiments of the present invention provide a memory including at least one such memory cell, an electronic device including such a memory, and methods of integrating a memory cell and erasing a memory cell.

220-P0015